AMENDMENTS

IN THE CLAIMS:

Claims 1-8 (Canceled)

9. (Previously Presented) A method of fabricating a semiconductor device comprising:

forming PMOS devices on a semiconductor substrate with source regions, drain regions, and entire source to drain channel regions formed within the substrate along a first crystallographic orientation axis of the semiconductor substrate;

forming NMOS devices on the semiconductor substrate with source regions, drain regions, and entire source to drain channel regions formed within the substrate rotated by an offset angle from the source to drain channel regions of the PMOS devices to lie along a second crystallographic orientation axis of the semiconductor substrate;

applying a compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility; and

applying a tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility.

10. (Original) The method of claim 9, wherein the crystallographic orientation axis on which the PMOS devices are formed is <110> and wherein the semiconductor substrate is silicon.

11. (Original) The method of claim 9, wherein the crystallographic orientation axis on which the NMOS devices are formed is <100>.

12. (Original) The method of claim 9, wherein the offset angle with which the source to drain channel region of the NMOS devices are formed is 45 degrees.

13. (Original) The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises applying uniaxial compressive strain.

14. (Original) The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises applying biaxial compressive strain.

15. (Original) The method of claim 9, wherein applying the compressive strain longitudinally across the source to drain channel regions of the PMOS devices to improve hole mobility comprises:

performing a recess etch of the source to drain channel regions; and

depositing a silicon-germanium epitaxial layer on the source to drain channel regions to introduce the compressive stress to the source to drain channel regions.

16. (Original) The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises applying biaxial tensile stress.

17. (Original) The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to improve electron mobility comprises:

performing a recess etch of the source to drain channel regions; and

depositing a carbon doped silicon layer on the source to drain channel regions to introduce the tensile stress to the source to drain channel regions.

18. (Original) The method of claim 9, wherein applying the tensile strain longitudinally across the source to drain channel regions of the NMOS devices to

improve electron mobility comprises forming an interlayer dielectric layer over the NMOS devices to introduce the compressive stress to the source to drain channel regions.

Claims 19-23 (Canceled)